High Definition Audio SoundMAX® Codec

AD1984

FEATURES

FOUR 192 kHz DACs/ADCs

Two independent stereo DAC/ADC pairs
Simultaneous record of two stereo channels
Simultaneous playback of two stereo channels
Independent 8, 11.025, 16, 22.05, 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz sample rates
16, 20, and 24-bit resolution
Selectable stereo mixer on outputs

4-CHANNEL DIGITAL MICROPHONE INTERFACE

Four 192 kHz digital microphone channels
Supports multiple microphone types
  Two microphones per pin (four total)
  One microphone per pin (two total)
Low pin count, uses 3 pins
Stereo or quad array support
8, 11.025, 16, 22.05, 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz sample rates
16, 20, and 24-bit resolution

S/PDIF OUTPUT

Supports 44.1, 48, 88.2, 96, 176.4, and 192 kHz sample rates
16, 20, and 24-bit data; PCM, and AC3 formats
Digital PCM gain control

DEDICATED AUXILLARY PINS

Stereo CD/auxillary I/O port w/GND sense
Stereo auxillary/dock I/O port
Mono out pin for internal speakers or telephony

ENHANCED FEATURES

Two stereo headphone amplifiers
Microsoft Vista premimum logo for notebook and desktop
  96+ dB audio outputs, 90+ dB audio inputs
Internal 32-bit arithmetic for greater accuracy
Impedance and presence detection on all jacks
Three independent microphone bias pins
Digital and analog PCBeep
Three general-purpose digital I/O (GPIO) pins
3.3 V analog and digital supply voltages
Advanced power management modes
48-lead, Pb-free LFCSP_VQ package

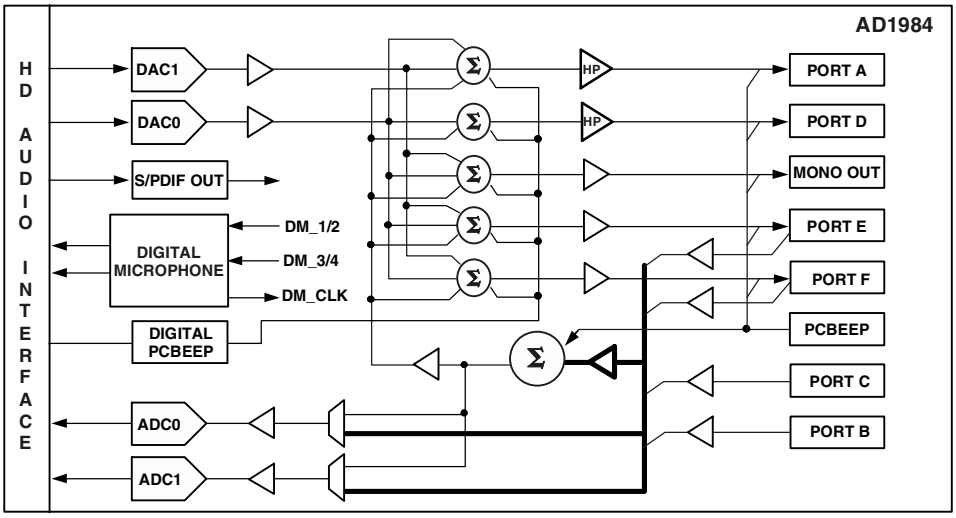

Figure 1. Functional Block Diagram

Rev. 0

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REVISION HISTORY

1/07–Rev 0: Initial version

GENERAL DESCRIPTION

The AD1984 family of audio codecs and SoundMAX® software provides superior High Definition audio quality that exceeds Vista Premium performance. The AD1984 has four 192 kHz DACs, four 192 kHz ADCs, S/PDIF output, a four-channel digital microphone interface, Digital Beep and analog PCBeep. These features make the AD1984 the right choice for desktop and notebook PCs where performance is key.

The AD1984 is available in a 48-lead, Pb-free frame chip scale package in both reels and trays. See Ordering Guide on Page 20.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the AD1984 SoundMAX codec's architecture and functionality. Additional information on the AD1984 is available in the AD1984 Programmers Reference Manual. Please contact your local ADI sales representitive for more information. For information on SoundMAX codecs and software see Analog Devices website at http://www.analog.com/soundMAX.

JACK CONFIGURATIONS

The guideline shown in Table 1 should be used when selecting ports for particular functions. The symbols used in this table are defined as: LI = Line Level Input, LO = Line Level Output, HP = Output capable of driving headphone load, MIC = Input supports microphones with MIC bias and boost amplifier.

Table 1. Port Assignments

Port	HP	MIC	LO	LI
Port A	x		x	
Port B		x		x
Port C		x		x
Port D	x		x	
Port E		x	x	x
Port F			x	x
MONO_OUT			x	

AD1984 SPECIFICATIONS

TEST CONDITIONS

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate F_S	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	–3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC	10 kΩ Output Load: Line Out tests
	32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

PERFORMANCE

Parameter	Min	Typ	Max	Unit
Line Out Drive (10 kΩ loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–86		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		96		dB
Signal-to-Noise Ratio		96		dB
Headphone Drive (32 Ω loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–80		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		96		dB
Signal-to-Noise Ratio		96		dB
Microphone/Line In (Pin to ADC, Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		–81		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		90		dB
Signal-to-Noise Ratio		90		dB

GENERAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
DIGITAL DECIMATION AND INTERPOLATION FILTERS[1]				
Pass Band – f_S (kHz) = 8 ~ 192	0		0.4 f_S	Hz
Pass-Band Ripple– f_S (kHz) = 8 ~ 192			±0.005	dB
Stop Band – f_S (kHz) = 8 ~ 192	0.6 f_S			Hz
Stop-Band Rejection – f_S (kHz) = 8 ~ 192			–100	dB
Group Delay – f_S (kHz) = 8 ~ 192		20		$1/f_S$
Group Delay Variation Over Pass Band		0		µs
ANALOG-TO-DIGITAL CONVERTERS				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[2]			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)		±0.2	±0.5	dB
ADC Offset Error[1]			±5	mV
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–85		dB
Line_In to Other		–100	–80	dB

Parameter		Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Resolution			24		Bits
Gain Error (Full Scale Span Relative to Nominal Input Voltage)[1]				±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)				±0.5	dB
Total Audible Out-of-Band Energy (Measured from 0.6 × f_S to 20 kHz)[1]			–85		dB
DAC Crosstalk (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)[1]			–95		dB
DAC VOLUMES					
Step size (DAC-0, DAC-1)			1.5		dB
Output Gain/Attenuation Range		–58.5		0	dB
Mute Attenuation of 0 dB Fundamental[1]			–80		dB
ADC VOLUMES					
Step size (ADCSEL-0, ADCSEL-1)			1.5		dB
PGA Gain/Attenuation Range		–58.5		+22.5	dB
ANALOG MIXER					
Signal-to-Noise Ratio Input to Output – Ports B, C, or F, to Port D Output			95		dB
Step Size: All Mixer Inputs			–1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		–34.5		+12.0	dB
ANALOG LINE LEVEL OUTPUTS					
Full-Scale Output Voltage: Line out drive enabled		1.0			V rms[3]
Ports A, D, E, F, and Mono Out		2.83			V p-p
	Output Impedance[1]		190		Ω
	External Load Impedance[1]	10			kΩ
	Output Capacitance[1]		15		pF
	External Load Capacitance			1000	pF
ANALOG HP DRIVE OUTPUTS					
Full-Scale Output Voltage: Line Out Drive Enabled		1.0			V rms[3]
Ports A and D (when HP Drive is Enabled)		2.83			V p-p
	Output Impedance[1]			0.5	Ω
	External Load Impedance[1]	32			Ω
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG INPUTS					
Input Voltages – Ports B, C, or E					
	Mic Boost = 0 dB		1		V rms[3]
			2.83		V p-p
Input Voltages – Microphone Boost	Mic Boost = +10 dB		0.316		V rms[3]
Amplifier, Ports B, C, or E			0.894		V p-p
	Mic Boost = +20 dB		0.1		V rms[3]
			0.283		V p-p
	Mic Boost = +30 dB		0.032		V rms[3]
			0.089		V p-p
Input Impedance					
PCBEEP			23		kΩ
Ports B, C, E (Mic Boost = 0 dB)			150		kΩ
Port F			45		kΩ
Input Capacitance[1]			5	7.5	pF

Parameter		Min	Typ	Max	Unit
MICROPHONE BIAS					
MIC_BIAS-B, MIC_BIAS-C					
MIC_BIAS_IN (Pin 33) = +5 V or +3.3 V	V_{REF} Setting = Hi-Z		Hi-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
MIC_BIAS_IN (Pin 33) = +5 V	V_{REF} Setting = 80%		3.7		V dc
	V_{REF} Setting = 100%		3.9		V dc
MIC_BIAS_IN (Pin 33) = +3.3 V	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
MIC_BIAS-E (When enabled as BIAS)	V_{REF} Setting = Hi-Z		Hi-Z		V dc
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
Output Drive Current	V_{REF} Setting = 50%, 80%, or 100%		1.6		mA
GPIO 0					
Input Signal High (V_{IH})		$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})		0		$DV_{IO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{IO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			–150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
GPIO 1 and 2					
Input Signal High (V_{IH})		$AV_{DD} \times 0.60$		AV_{DD}	V
Input Signal Low (V_{IL})		0		$AV_{DD} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$AV_{DD} \times 0.72$		AV_{DD}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$AV_{DD} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			–150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
DM Clock					
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$AV_{DD} \times 0.72$		AV_{DD}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$AV_{DD} \times 0.10$	V
DM 1/2 and 3/4					
Input Signal High (V_{IH})		$AV_{DD} \times 0.60$		AV_{DD}	V
Input Signal Low (V_{IL})		0		$AV_{DD} \times 0.24$	V
Input Leakage Current (Signal High) (I_{IH})			–150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		nA
POWER SUPPLY					
Analog (AV_{DD}) 3.3 V ±5%					
Power Supply Range		3.13	3.30	3.46	V
Power Dissipation			99		mW
Supply Current			31		mA
Digital (DV_{DD}) 3.3 V ±10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			162		mW
Supply Current			58		mA
Digital I/O (DV_{IO}) 3.3 V ±10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.96		mW
Supply Current			1.2		mA
Power Supply Rejection (reference to f_S 100 mV p-p Signal @ 1 kHz)[1]			80		dB

[1] Guaranteed but not tested.
[2] Measurements reflect main ADC.
[3] RMS values assume sine wave input.

HD–AUDIO LINK SPECIFICATION

High-definition audio signals comply with the High-definition Audio specification. Please refer to these specifications at: *http://www.intel.com/standards/hdaudio/*

POWER DOWN STATES

Parameter	ID_{VDD} Typ	IA_{VDD} Typ	Unit
Function node in D0, all nodes active	58	31	mA
Function node in D3[1]	21	2	mA
Codec in $\overline{\text{RESET}}$	3	3	mA
Individual block power savings			
DAC pair powered down saves (each)	6	5	mA
ADC pair powered down saves (each)	5	3	mA
Mixer power control (and associated amps) saves	0	2	mA
DM_FLT pair powered down saves (each)	5	0	mA
DM_CLK powered down saves[2]	0	1	mA
MIC_BIAS powered down saves[3]	0	0.5	mA

[1] Function node D3 state powers down all nodes except for the V_{REF}, Mixer and MIC_BIAS nodes which have independent power controls. V_{REF} should be kept active when background functions such as jack presence detection or analog pass-through are required. Mixer should be kept active when analog pass-through is required. MIC_BIAS can be disabled if microphones are not in use in the power-down state.

[2] Test conditions: 30 pF load, 2.0 MHz frequency, 3.3 V $A_{VDD.}$

[3] Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits set to 100% or 50%, setting them to the Hi-Z state. The 0 Ω and Hi-Z states remain unaffected by the MIC_BIAS power state.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Supplies	Min	Max	Unit
Digital (DV_{DD})	–0.30	+3.65	V
Digital I/O (DV_{IO})	–0.30	+3.65	V
Analog (AV_{DD})	–0.30	+3.65	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.30	AV_{DD} + 0.3	V
Digital Input Voltage (Signal Pins)	–0.30	DV_{IO} + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	–65	+150	°C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be take to avoid performance degradation or loss of functionality.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} – (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Table 2. Thermal Resistance

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
LFCSP_VQ	47	15	32	°C/W

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

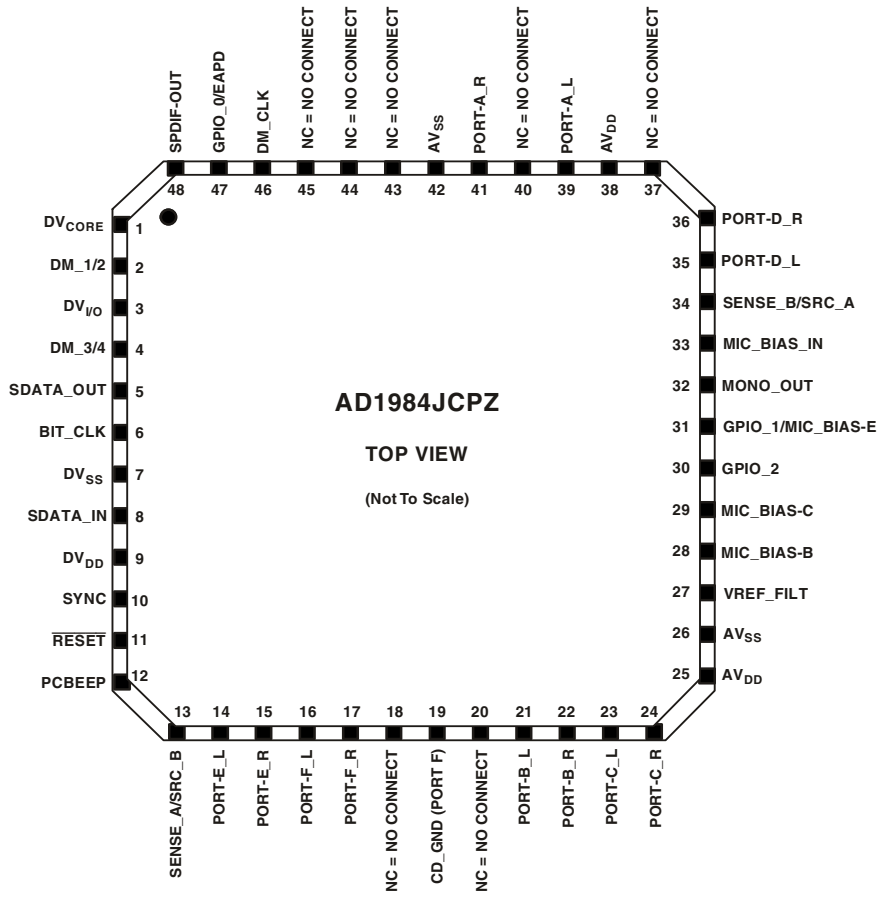

Figure 2. AD1984 48-Lead Package and Pinout

Table 3. AD1984 Pin Descriptions

Mnemonic	Pin No.	I/O	Description
DIGITAL INTERFACE			
SDATA_OUT	5	I	Link Serial Data Output. AD1984 input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock .
SDATA_IN	8	I/O	Link Serial Data Input. AD1984 output stream clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
$\overline{\text{RESET}}$	11	I	Link Reset. AD1984 master hardware reset.
DIGITAL I/O			
DM_1/DM_2	2	I	Digital microphone 1 and 2 inputs (for bi-phase microphones), or digital microphone 1 input (for single-phase microphones).
DM_3/DM_4	4	I	Digital microphone 3 and 4 inputs (for bi-phase microphones), or digital microphone 2 input (for single-phase microphones).
DM_CLK	46	O	Clock to drive external digital microphones.
GPIO_2	30	I/O	General Purpose Input/Output Pins. Digital signals used to control or sense external circuitry.
GPIO_1/MIC_BIAS-E	31	I/O	General Purpose I/O/Microphone Bias for Port E. Capable of Hi-Z, 1.65 V, and 2.86 V. Pin 31 shares functionality between GPIO_1 (default) and MIC_BIAS_E. These functions are mutually exclusive and the GPIO function takes priority over the MIC_BIAS function. When the GPIO enable bit is 0, Pin 31 functions as a MIC_BIAS pin associated with Port E.
GPIO_0/EAPD	47	I/O	EAPD/General Purpose Input/Output pin. Pin 47 shares functionality between GPIO_0 and EAPD. These functions are mutually exclusive and the EAPD function takes priority over the GPIO function. By default, the pin is in a Hi-Z state. External resistors should be used to insure the proper circuit state when this pin is in Hi-Z.
S/PDIF_OUT	48	O	S/PDIF_OUT – Supports S/PDIF output.
JACK SENSE AND EAPD			
SENSE_A/SRC_B	13	I/O	Jack Sense A-D Input/Sense B drive.
SENSE_B/SRC_A	34	I/O	Jack Sense E-F Input/Sense A drive.
ANALOG I/O			
PCBEEP	12	LI	Monaural Input from system for Analog PCBeep.
Port E_L	14	LI, MIC, LO	Auxiliary Input/Output Left Channel.
Port E_R	15	LI, MIC, LO	Auxiliary Input/Output Right Channel.
Port F_L	16	LI, LO	Auxiliary Input/Output Left Channel.
Port F_R	17	LI, LO	Auxiliary Input/Output Right Channel.
CD_GND	19	I	CD-Audio-Analog-Ground-Reference. Must be connected to AGND via a 0.1 µF capacitor if not in use as CD_GND. MUST always be ac coupled.
Port B_L	21	LI, MIC	Front Panel Stereo MIC/Line-In.
Port B_R	22	LI, MIC	Front Panel Stereo MIC/Line-In.
Port C_L	23	LI, MIC	Rear Panel Stereo MIC/Line-In.
Port C_R	24	LI, MIC	Rear Panel Stereo MIC/Line-In.
MONO_OUT	32	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
Port D_L	35	HP, LO	Rear Panel Headphone/Line-Out.
Port D_R	36	HP, LO	Rear Panel Headphone/Line-Out.
Port A_L	39	HP, LO	Front Panel Headphone/Line-Out.
Port A_R	41	HP, LO	Front Panel Headphone/Line-Out.

The symbols used in this table are defined as: I = Input, O = Output, LI = Line Level Input, LO = Line Level Output, HP = Output capable of driving headphone load, MIC = Input supports microphones with MIC bias and boost amplifier.

Table 3. AD1984 Pin Descriptions (Continued)

Mnemonic	Pin No.	I/O	Description
FILTER/REFERENCE			
V_{REF} _FILT	27	O	Voltage Reference Filter.
MIC_BIAS-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24). Both MIC bias pins are capable of Hi-Z, 0 V, 1.65 V, 3.7 V, and 3.9 V (with 5.0 V on Pin 33), Hi-Z, 0 V, 1.65 V, 2.86 V, and 3.0 V (with 3.3 V on Pin 33).
DV_{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. This pin must be connected to filter caps: 10 µF, 1.0 µF, and 0.1µF connected in parallel between Pin 1 and D_{VSS} (Pin 7).
POWER AND GROUND			
DV_{IO} 3.3V	3	I	Link Digital I/O Voltage Reference. 3.3 V
DV_{SS}	7	I	Digital supply return (ground).
DV_{DD} 3.3 V	9	I	Digital supply voltage 3.3 V . This is regulated down to DV_{CORE} on Pin 1 to supply the internal digital core internal to the AD1984.
AV_{DD} 3.3 V	25, 38	I	CAUTION: DO NOT APPLY 5 V TO THESE PINS! Analog supply voltage 3.3 V ONLY. Note: AV_{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN 5.0 V or 3.3 V	33	I	Source power for microphone bias boost circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way the AD1984 is capable of providing +3.9 V as a mic bias to all of the mic bias pins (except on Pin 31). If 5 V is not available, connect this pin to +3.3 V (AV_{DD}) via a low-pass filter. The AD1984 produces a mic bias voltage relative to the AV_{DD} supply (typically 3.0 V @ AV_{DD} = 3.3 V).
AV_{SS}	26, 42	I	Analog supply return (ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1984.

The symbols used in this table are defined as: I = Input, O = Output, LI = Line Level Input, LO = Line Level Output, HP = Output capable of driving headphone load, MIC = Input supports microphones with MIC bias and boost amplifier.

DIGITAL MICROPHONE INTERFACE TIMING SPECIFICATIONS

The digital microphone interface can support one, two, or four digital microphones using two or three codec pins. Both uniplex (one mic per data pin) and multiplex (two mics sharing the same data pin) are supported. These configurations are shown in Figure 3, Figure 4, Figure 6, and Figure 7. The interface can generate a microphone clock at 1.5 MHz, 2.0 MHz, or 3.0 MHz to suit quality and power requirements.

Table 4. Digital Microphone Timing Parameters

Parameter		Min	Typ	Max	Unit
Timing Requirements					
t_0	DM_CLK (1.5 MHz) Period		667		ns
	Duty Cycle		60/40		%
t_0	DM_CLK (2.0 MHz) Period		500		ns
	Duty Cycle		50/50		%
t_0	DM_CLK (3.0 MHz) Period		333		ns
	Duty Cycle		50/50		%
t_1	DM_CLK Rise Time			5	ns
t_2	DM_CLK Fall Time			5	ns
t_3	DM_CLK Edge to Data Valid		40		ns
t_4	Data Setup to DM_CLK Edge	100			ns
t_5	Data Hold from DM_CLK Edge	5			ns
t_6	DM_CLK Edge to Data Hi-Z		7		ns

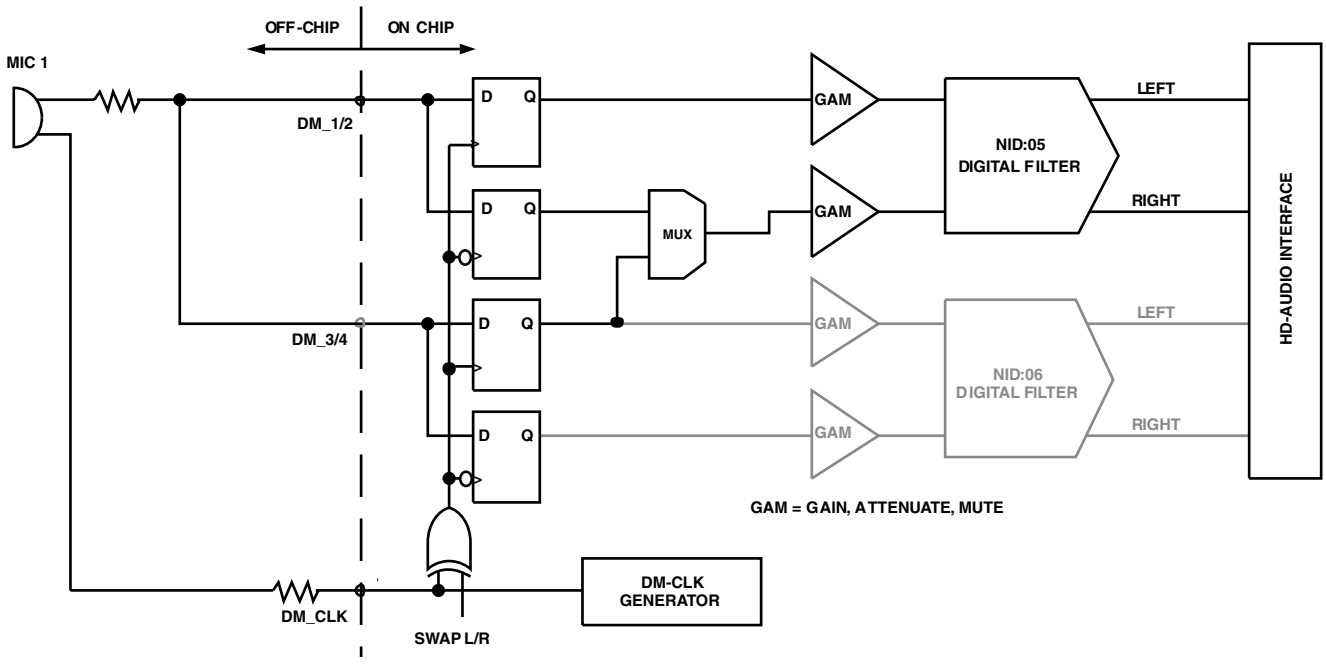

Figure 3. Uniplex Digital Microphone, Mono Interface

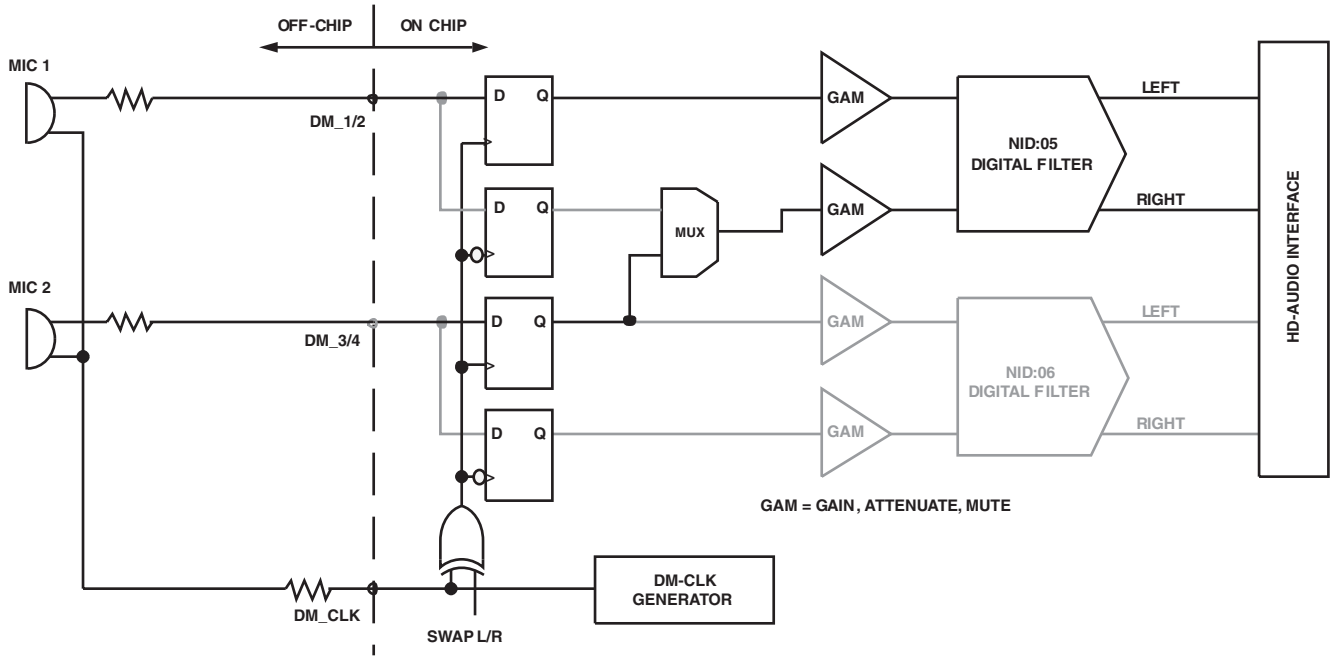

Figure 4. Uniplex Microphone, Stereo Interface

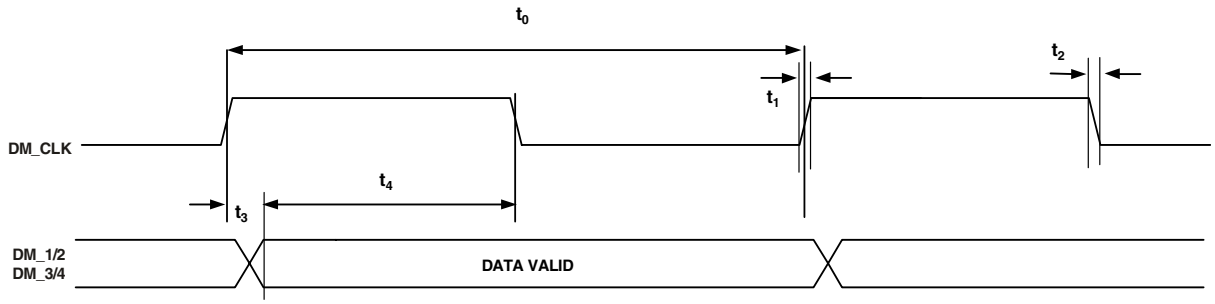

Figure 5. Uniplex Microphone Timing

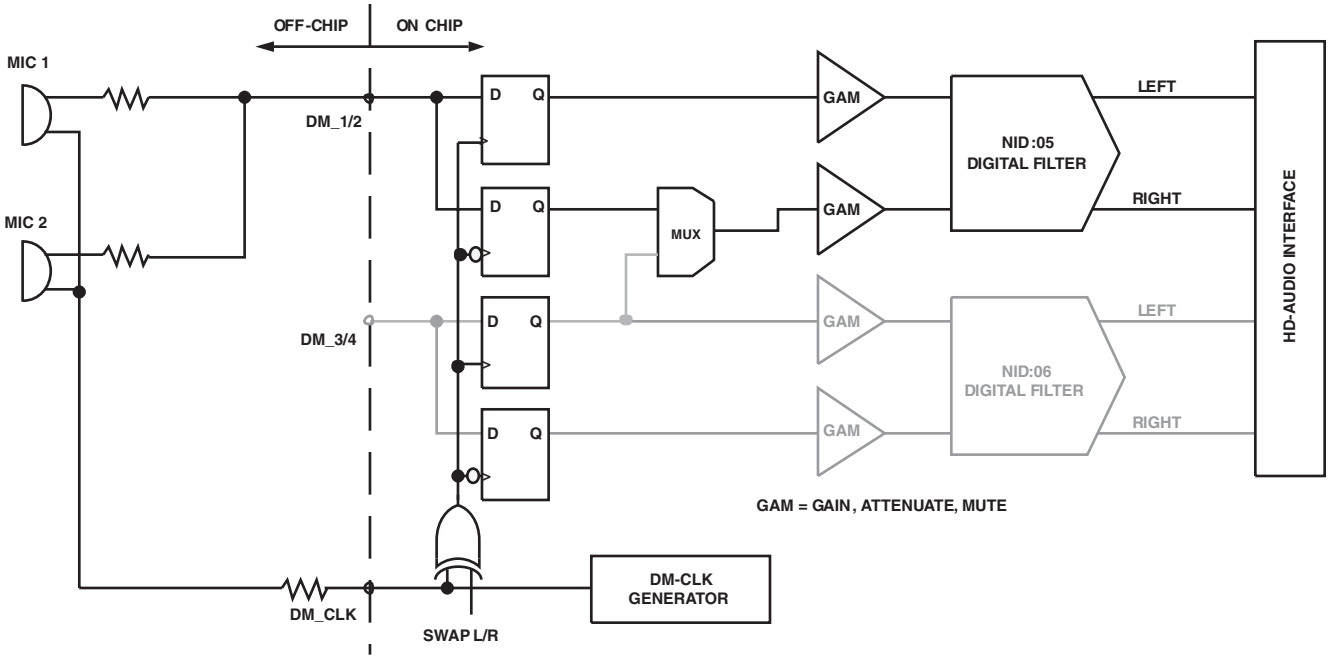

Figure 6. Multiplex Digital Microphone, Stereo Interface

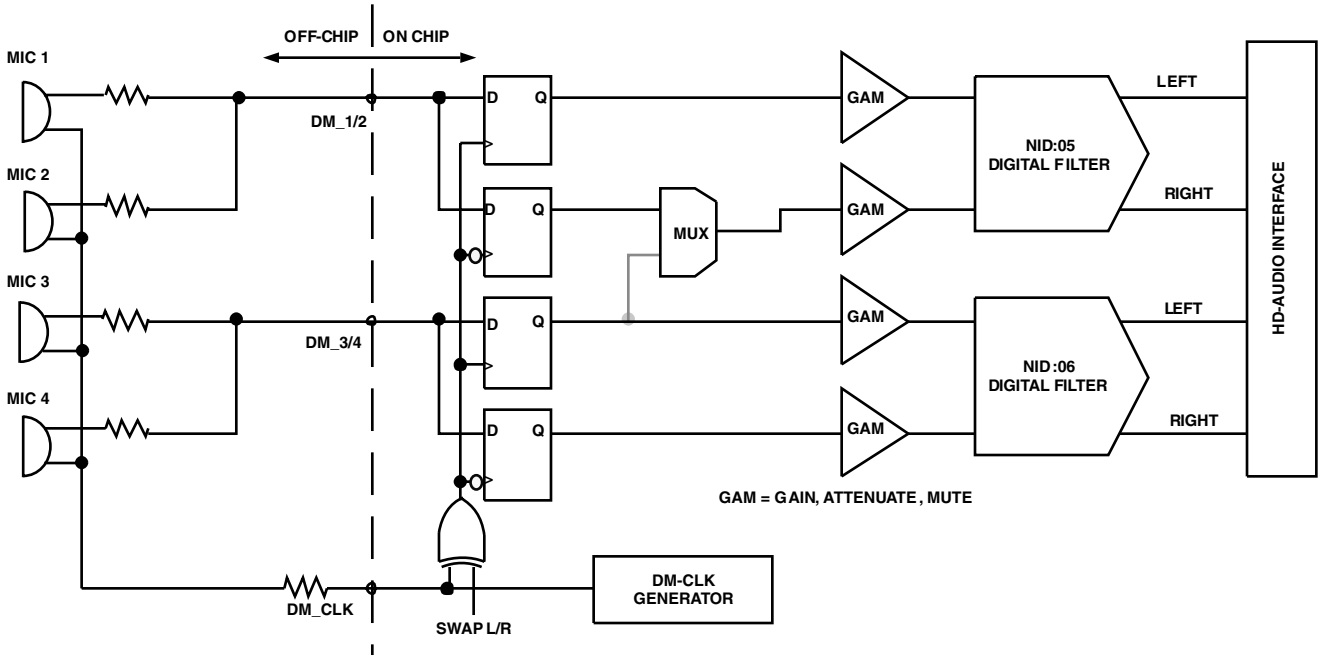

Figure 7. Multiplex Digital Microphone, Quad Interface

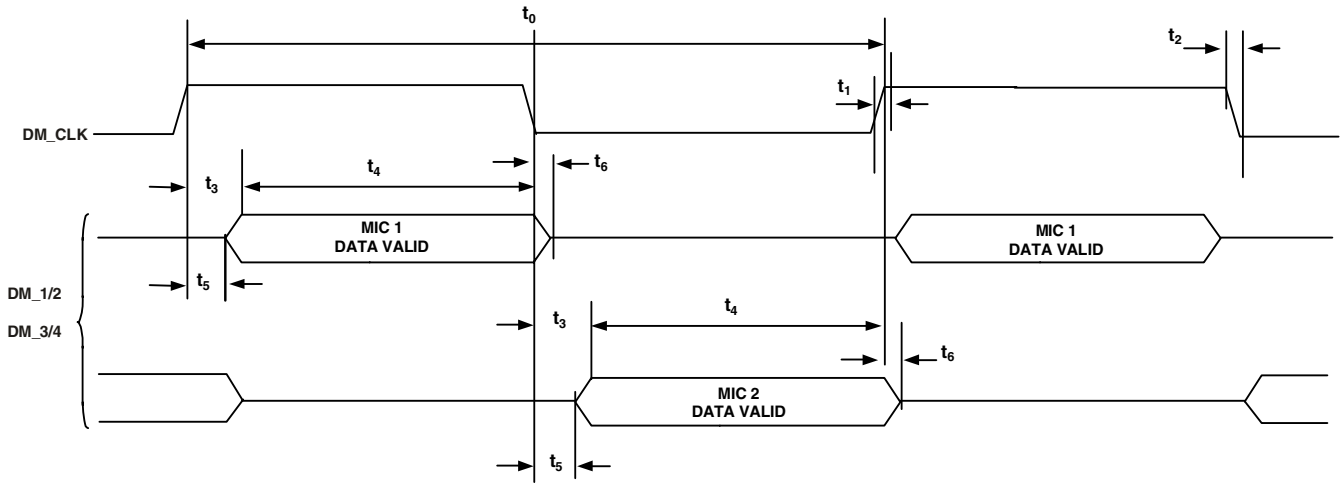

Figure 8. Multiplex Microphone Timing

HD AUDIO WIDGETS

Table 5. HD Audio Widgets

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device identification
01	FUNCTION	x	Function	Designates this device as an audio CODEC
02	S/PDIF DAC	0	Audio Output	S/PDIF digital stream output interface
03	DAC_0	0	Audio Output	Stereo headphone channel digital/audio converters
04	DAC_1	0	Audio Output	Stereo front channel digital/audio converters
05	Dig Mic Conv 1/2	1	Audio Input	Digital microphone Channel 1, 2 converters
06	Dig Mic Conv 3/4	1	Audio Input	Digital microphone Channel 3, 4 converters
07	Port A Mixer	2	Audio Mixer	Mixes the of DAC_(0, 1) and mixer output amps to drive Port A
08	ADC_0	1	Audio Input	Stereo record Channel 0 audio/digital converters
09	ADC_1	1	Audio Input	Stereo record Channel 1 audio/digital converters
0A	Port D Mixer	2	Audio Mixer	Mixes the DAC_1 and mixer output amps to drive Port D
0B	Port F Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and mixer output amps to drive Port F
0C	ADC Selector 0	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_0
0D	ADC Selector 1	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_1
0E	Mono Out Selector	3	Audio Selector	Selects the mono out DAC_(0, 1)
0F	Port F Out Selector	3	Audio Selector	Selects the Port F DAC_(0, 1)
10	Digital Beep	7	Beep Generator	Internal digital PCBeep signal
11	Port A (Headphone)	4	Pin Complex	Headphone jack pins
12	Port D (Line Out)	4	Pin Complex	Line out jack pins
13	Mono Out	4	Pin Complex	Monaural output pin (internal speakers or telephony system)
14	Port B (Mic In)	4	Pin Complex	Microphone in jack pins
15	Port C (Line In)	4	Pin Complex	Line in jack pins
16	Port F (Aux In/Out)	4	Pin Complex	Auxiliary I/O pins
17	Dig Mic 1/2 Pin	4	Pin Complex	Digital microphone 1, 2 input pin
18	Dig Mic 3/4 Pin	4	Pin Complex	Digital microphone 3, 4 input pin
19	Mixer Power Down	5	Power Widget	Powers down the analog mixer and associated amps
1A	Analog PCBeep	4	Pin Complex	External analog PCBeep signal input
1B	S/PDIF Out Pin	4	Pin Complex	S/PDIF output pin
1C	Port E (Dock I/O)	4	Pin Complex	Analog dock I/O pins
1D	V_{REF} Power Down	F	Vendor Defined	Powers down the internal and external V_{REF} circuitry
1E	Mono Out Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and mixer output amps to drive mono out
1F	Stereo Mix-Down	2	Audio Mixer	Mixes the stereo L/R channels to drive mono output
20	Analog Mixer	2	Audio Mixer	Mixes individually gainable analog inputs
21	Mixer Output Atten	3	Audio Selector	Attenuates the mixer output to drive the port mixers
22	Port A Out Selector	3	Audio Selector	Selects the Port A DAC_(0, 1)
23	Port E Out Selector	3	Audio Selector	Selects the Port E DAC_(0, 1)
24	Port E Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and mixer output amps to drive Port E
25	Port E Mic Boost	3	Audio Selector	0 dB, 10 dB, 20 dB, or 30 dB gain boost for Port E
26	BIAS Power Down	F	Vendor Defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS pins

AD1984 HD AUDIO PARAMETER

Table 6. Root and Function Node Parameters

Node ID	Name	Type	Vendor ID 00	Revision ID 02	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	Root	11D41984	00100400	00010001			
01	FUNCTION	Function			00020025	00000001	00010C0C	40000003

Table 7. SubSystem ID [1]

		31:16	15:8	7:0
		SSID	SKU	Asm ID
01	FUNCTION	BFD4	00	00

[1] The SSID value is set on codec power-up only. SSID is not reset by link or soft reset in order to preserve modifications by BIOS control.

Table 8. Widget Parameters

Node ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	Con. List Length 0E	Power States 0F	Output Amp Capabilities 12
01	000004C0	000E07FF	00000001		80000000		00000009	00052727
02	00030311	000E07E0	00000005			00000003		
03	00000405	000E07FF	00000001			00000000	00000009	00052727
04	00000405	000E07FF	00000001			00000000	00000009	00052727
05	0010050B	000E07FF	00000001		80053627	00000001	00000009	
06	0010050B	000E07FF	00000001		80053627	00000001	00000009	
07	00200103				80000000	00000002		
08	00100501	000E07FF	00000001			00000001	00000009	
09	00100501	000E07FF	00000001			00000001	00000009	
0A	00200103				80000000	00000002		
0B	00200103				80000000	00000002		
0C	0030010D					00000004		80053627
0D	0030010D					00000004		80053627
0E	00300101					00000002		
0F	00300101					00000002		
10	0070000C					00000000		800B0F0F
11	0040018D			0000001F		00000001		80000000
12	0040058D			0001001F		00000001	00000009	80000000
13	0040050C			00010010		00000001	00000009	80051F1F
14	0040008B			00003727	00270300	00000000		
15	0040008B			00003727	00270300	00000000		
16	0040018D			00000037		00000001		80000000
17	00400001			00000020		00000000		
18	00400001			00000020		00000000		
19	00500500					00000002	00000009	
1A	00400000			00000020		00000000		
1B	0040030D			00000010		00000001		80052727
1C	0040018D			00003737		00000001		80000000
1D	00F00100					0000000A		
1E	00200103				80000000	00000002		
1F	00200100					00000001		
20	0020010B				80051F17	00000004		
21	0030010D					00000001		80051F1F
22	00300101					00000002		

Table 8. Widget Parameters (Continued)

Node ID	Widget Capabilities 09	PCM Size, Rate 0A	Stream Formats 0B	Pin Capabilities 0C	Input Amp Capabilities 0D	Con. List Length 0E	Power States 0F	Output Amp Capabilities 12
23	00300101					00000002		
24	00200103				80000000	00000002		
25	0030010D					00000001		00270300
26	00F00100					00000003		

Table 9. Connection List

Node	Connections			0		1		2		3		4		5		6		7		8		9	
ID	[0–3]	[4–7]	[8–11]	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID	I	NID
02	00090801				01		08	I	09														
03																							
04																							
05	00000017				17																		
06	00000018				18																		
07	00002122				03		21																
08	0000000C				0C																		
09	0000000D				0D																		
0A	00002104				04		21																
0B	0000210F				0F		21																
0C	25209614			1	14		16		20		25												
0D	25209614			1	14		16		20		25												
0E	00000403				03		04																
0F	00000403				03		04																
10																							
11	00000007				07																		
12	0000000A				0A																		
13	0000001F				1F																		
14																							
15																							
16	0000000B				0B																		
17																							
18																							
19	00002120				20		21																
1A																							
1B	00000002				02																		
1C	00000024				24																		
1D	8F0A1907	96111C1A	0000A61E		07		19		0A	1	0F		1A		1C		11	1	16		1E	1	26
1E	0000210E				0E		21																
1F	0000001E				1E																		
20	251A9614			1	14		16		1A		25												
21	00000020				20																		
22	00000403				03		04																
23	00000403				03		04																
24	00002123				23		21																
25	0000001C				26																		
26	001C1514				14		15																

In Table 10, default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control. Bits 11:9 are reserved.

Table 10. Default Configuration Bytes

			31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
				Location							
ID	Name	Value	Connectivity	Chasis	Position	Def. Device	Conn Type	Color	JD OR	Def Assn.	Seq.
11	Port A	0321401F	Jack	External	Left	HP Out	1/8" Jack	Green	0	1	F
12	Port D	90130110	Fixed	Internal	N/A	Speaker	ATAPI	Unknown	1	1	0
13	Mono Out	901301F0	Fixed	Internal	N/A	Speaker	ATAPI	Unknown	1	F	0
14	Port B	03A190F0	Jack	External	Left	Mic In	1/8" Jack	Pink	0	F	0
15	Port C	96A30120	Fixed	Internal	Bottom	Mic In	ATAPI	Unknown	1	2	0
16	Port F	99330121	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	1
17	Dig Mic 1/2 Pin	95A601F0	Fixed	Internal	Top	Mic In	Other Digital	Unknown	1	F	0
18	Dig Mic 3/4 Pin	95A601F0	Fixed	Internal	Top	Mic In	Other Digital	Unknown	1	F	0
1A	Analog PCBeep	90F301F0	Fixed	Internal	N/A	other	ATAPI	Unknown	1	F	0
1B	S/PDIF Out Pin	014511F0	Jack	External	Rear	SPDIF Out	Optical	Black	1	F	0
1C	Port E	21A1902E	Jack	Separate	Rear	Mic In	1/8" Jack	Pink	0	2	E

OUTLINE DIMENSIONS

Dimensions are shown in millimeters.

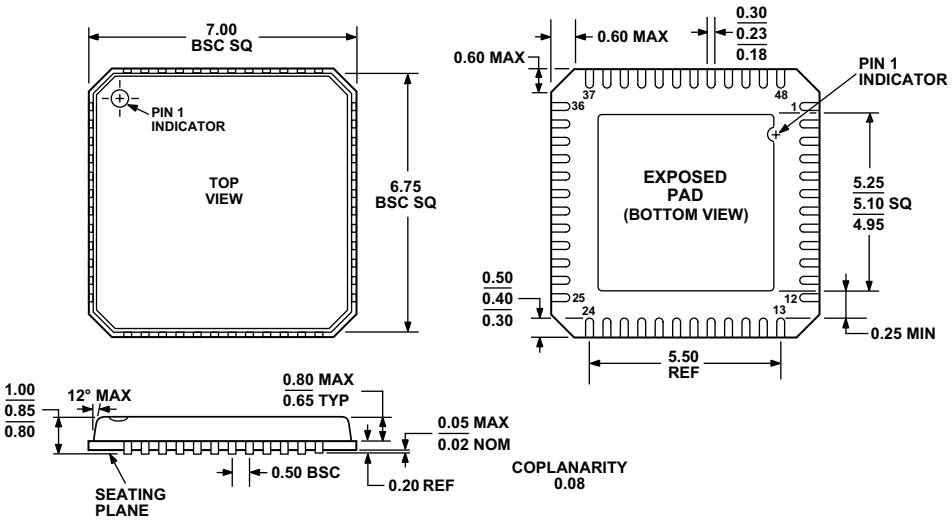

Figure 9. 48-Lead, Pb-Free, Frame Chip Scale Package [LFCSP_VQ]
7 mm x 7 mm Body, Very Thin Quad (CP-48-1)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1984JCPZ[1]	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1
AD1984JCPZ-REEL[1]	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1

[1] Z = Pb-free part.

D06535-0-1/07(0)